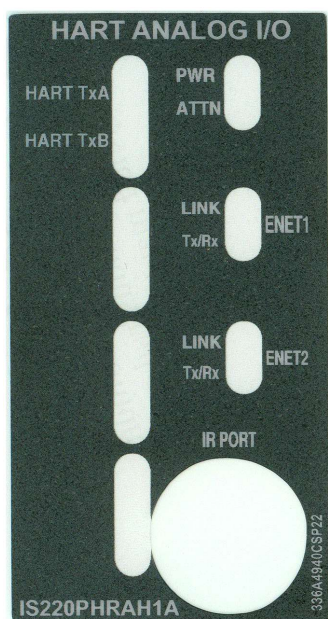


PHRA HART® Enabled Analog I/O Module

HART Enabled Analog Input/Output (PHRA)

Functional Description

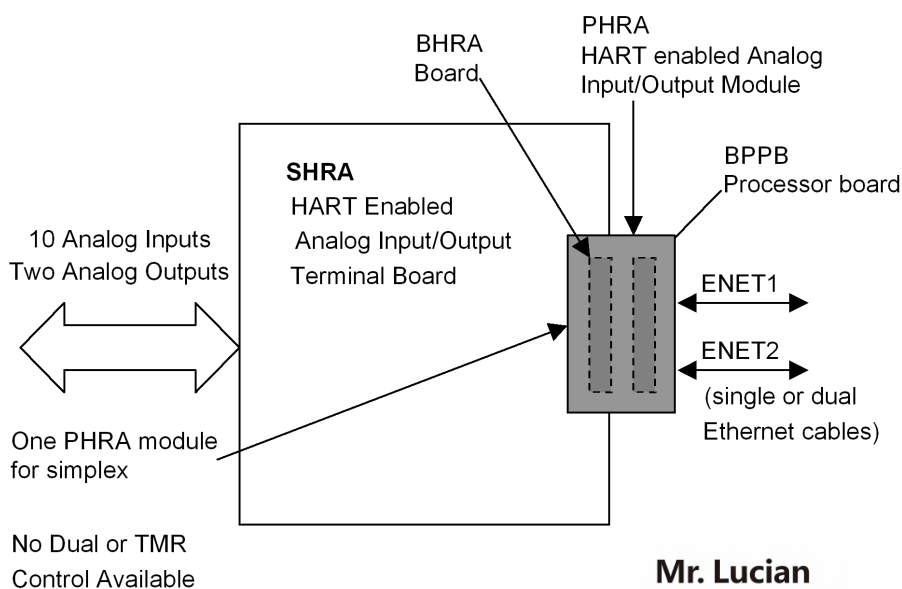


Infrared Port Not Used

The Highway Addressable Remote Transducer (HART®) Enabled Analog I/O pack (PHRA) provides the electrical interface between one or two I/O Ethernet networks and an analog input/output terminal board. The PHRA contains a processor board common to the distributed I/O packs and an acquisition board specific to the analog input function.

The I/O pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as ± 5 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ± 1 mA or 4-20 mA current inputs. The load termination resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the PHRA. The PHRA also includes support for two 4-20 mA current loop outputs. In addition, in 4-20 mA mode the PHRA can relay HART messages between HART enabled field devices and an Asset Management System (AMS). These HART enabled field devices can be connected through any of the inputs or outputs.

Input to the I/O pack is through dual RJ-45 Ethernet connectors and a 3-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



PHRA Block Diagram

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Installation

➤ To install the PHRA I/O pack

1. Securely mount the desired terminal board.
2. Directly plug one PHRA I/O pack into the terminal board connector.
3. Mechanically secure the pack using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.

Note The PHRA mounts directly to a SHRA simplex terminal board, which has a single DC-62 pin connector to receive the PHRA.

4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary.



Attention

If the configuration being downloaded contains I/O packs with different module IDs than the configuration currently running, the download can install incorrect firmware to some I/O packs. If this occurs, make sure the controller is running the new configuration, restart the entire system, and then start the ToolboxST Download Wizard again.

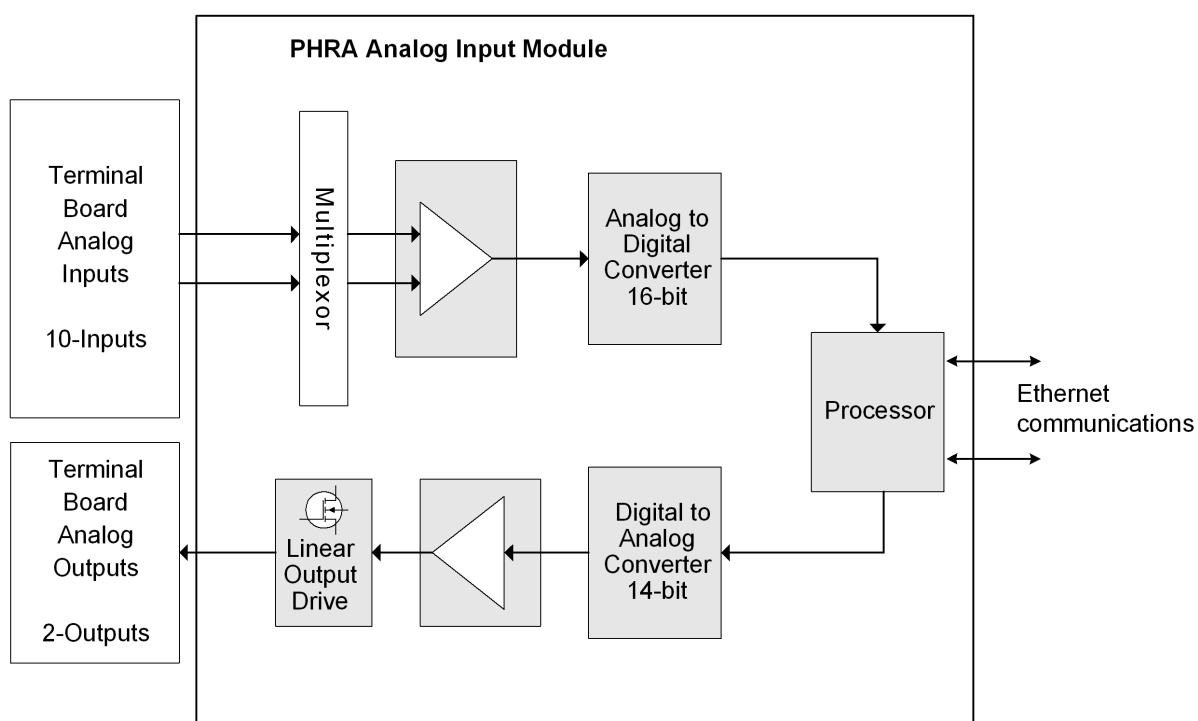
Operation

Refer to the following sections in the chapter, *Common Module Content*:

- [Auto-Reconfiguration](#)
- [Processor](#)
- [Processor LEDs](#)
- [ID Line](#)

Analog Input Hardware

The PHRA accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (DAC).

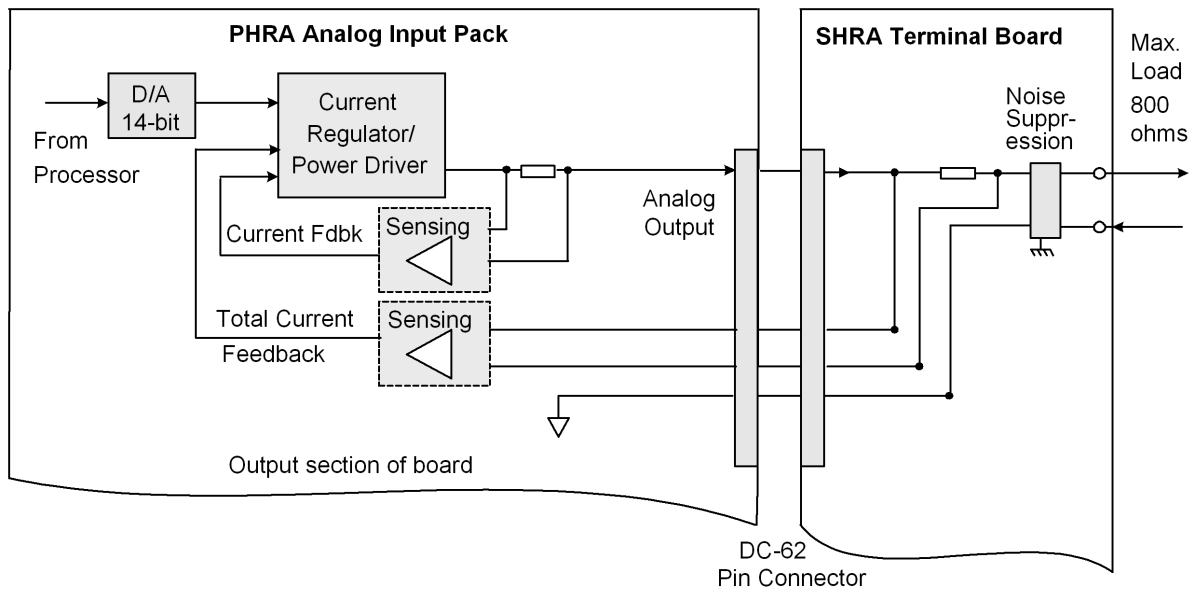


The inputs can be individually configured as ± 5 V scale signals, depending on the input configuration. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a second order, passive, low pass filter network with poles at 12.5 Hz and 48.3 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the PHRA analog input section.

Analog Output

The PHRA includes two 4-20 mA analog outputs capable of 18 V compliance. A 14-bit DAC commands a current reference to the current regulator loop in the PHRA that senses current both in the PHRA pack and on the terminal board. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the PHRA)
- Total current (as sensed from the terminal board)



HART Hardware

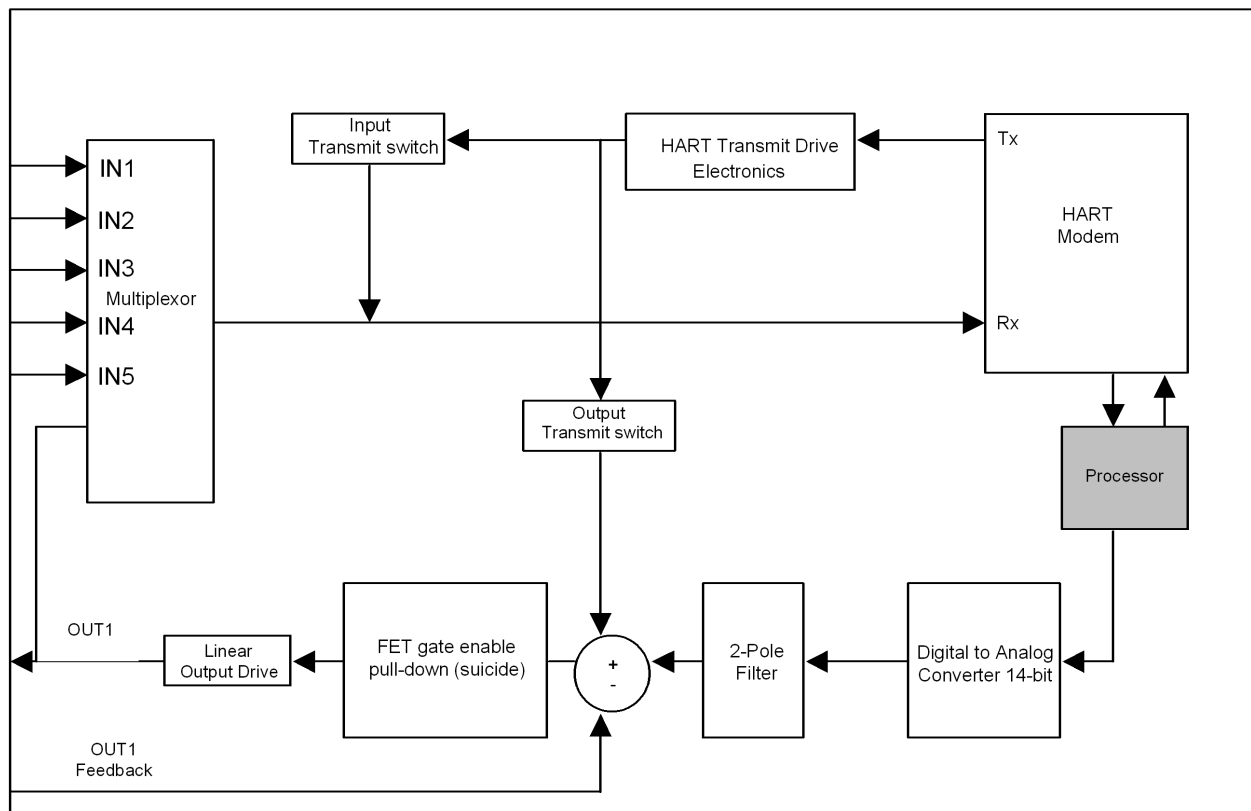
All inputs and outputs on the BHRA are HART enabled. This means there are 12 individual HART channels, with 10 channels for the analog inputs and two channels for the outputs. These 12 channels are served by a pair of HART modems so that each modem is associated with six HART channels. Inputs 1 through 5 and output 1 are multiplexed down to HART modem A. Inputs 6 through 10 and output 2 are multiplexed down to HART modem B.

HART Modem Associations

HART channel	PHRA I/O Analog	Served by Modem
1	Input #1	A
2	Input #2	A
3	Input #3	A
4	Input #4	A
5	Input #5	A
6	Output #1	A
7	Input #6	B
8	Input #7	B
9	Input #8	B
10	Input #9	B
11	Input #10	B
12	Output #2	B

Refer to the Network section
of GEH-6721, Vol I, Mark VIe
Control System Guide.

The number of active channels a modem is serving greatly impacts the HART data update time. If one of the six channels served by a HART modem is active, the modem is dedicated to a single field device and, under normal operating conditions, ToolboxST data associated with this device is updated roughly once per second. If all six channels are in use, roughly eight seconds will pass between updates.



Analog IO HART Interface — Quantity 2

Specifications

Item	Specification
Number of channels	12 channels per terminal board (10 AI, 2 AO)
Input span	4-20 mA dc, ± 5 V dc, (Inputs 1-8) 4-20 mA or ± 1 mA (Inputs 9-10)
Input converter resolution	16-bit analog-to-digital converter
Scan time	Normal scan 5 ms (200 Hz). Note that controller frame rate is 100 Hz.
Measurement accuracy	Better than 0.1% full scale over the temperature range 0 to 60°C. Typical accuracy at 25°C is 0.007% full scale.
Noise suppression on inputs	The ten circuits have a hardware filter with two poles at 12.5 Hz and 48.3 Hz. A software filter, using a two-pole, low-pass filter, is configurable for: 0, .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common mode rejection	Ac common mode rejection 60 dB at 60 Hz, with up to ± 5 V common mode voltage. Dc common mode rejection 80 dB with -5 to +7 peak V common mode voltage
Common mode voltage range	± 5 V
Output converter	14-bit D/A converter with 0.5% accuracy
Output load	800 Ω for 4-20 mA output
Physical	
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Temperature	-30 to 65°C (-22 to 149 °F)

Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG_XXXX, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RSTSYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAg signal if they go healthy.

Configuration

Note The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

Parameter	Description	Choices
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable (default-enable)
Min_MA_Input	Select minimum current for healthy 4-20 mA input	0 to 21 mA
Max_MA_Input	Select maximum current for healthy 4-20 mA input	0 to 21 mA
AMS_Msg_Priority	AMS messages have priority over controlled messages,	Enable, Disabled
AMS_Msgs_Only	AMS messages only, do not send any control messages. Generates alarm 160 when enabled.	Enable, Disabled
AMS_Mux_Scans_Permitted	Allow AMS scan commands for HART message 1 and 2. HART message 3 is always allowed	Enable, Disable
Max_MA_Hart_Output	Minimum current sent to a HART enabled port. HART COMM will not be possible during offline modes if value is set less than 4 mA	0-22.5
:IS200SHRA	Terminal board connected to PHRA	Connected, not connected
AnalogIn1-10	First of 10 Analog Inputs – board point	(Input FLOAT)
Input_Type	Current or voltage input type	Unused, 4-20 mA, ± 5 V
Low_Input	Value of current at the low end of scale	-10 to +20
Low_Value	Value of input in engineering units at low end of scale	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of current at the high end of scale	-10 to +20
High_Value	Value of input in engineering units at high end of scale	-3.4082 e + 038 to 3.4028 e + 038
Input_Filter	Bandwidth of input signal filter	Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_Ctrl	Number of variables to read from the device. Set to zero if not used.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected. (Right-click on device name and select Update HART IDS)	0-255
Hart_DevType	HART Field Device – Type of device. (See Hart_MfgID)	0-255

Parameter	Description	Choices
Hart_DeVID	HART Field Device – Device ID. (See Hart_MfgID)	0-116777215
Sys Lim 1 Enabl	Input fault check	Enable, disable
Sys Lim 1 Latch	Input fault latch	Latch, unlatch
Sys Lim 1 Type	Input fault type	≤ or ≥
Sys Lim 1	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
Sys Lim 2 Enabl	Input fault check	Enable, disable
Sys Lim 2 Latch	Input fault latch	Latch, unlatch
Sys Lim 2 Type	Input fault type	≤ or ≥
Sys Lim 2	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enable high input limit	Enable, disable
DiagLowEnab	Enable low input limit	Enable, disable
AnalogOut1-2	First of two analog outputs - board point	Point edit (Output FLOAT)
Output_MA	Type of output current, mA selection	Unused, 0-20 mA
Output_State	State of the outputs when offline	PwrDownMode Hold Last Value Output_Value
Output_Value	Pre-determined value for the outputs	
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in engineering units at low mA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in engineering units at high mA	-3.4082 e + 038 to 3.4028 e + 038
D/A Err Limit	Difference between D/A reference and output, in %	0 to 100 %
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_Ctrl	Number of variables to read from the device. Set to zero if not needed for control.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26
Update HART IDS	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected.	0-255
Hart_DeVType	HART Field Device – Type of device. (See Hart_MfgID)	0-255
Hart_DeVID	HART Field Device – Device ID. (See Hart_MfgID)	0-116777215

Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_PHRA	Board diagnostic	Input	BIT
LINK_OK_PHRA	Link diagnostic input	Input	BIT
ATTN_PHRA	Module diagnostic	Input	BIT
IOPackTmpr	I/O pack temperature	Input	FLOAT
PS18V_PHRA_R	I/O 18 V power supply indication	Input	BIT
PS28V_PHRA_R	I/O 28 V power supply indication	Input	BIT
MuxHealth1	Health bit for PHRA HART multiplexer	Input	BIT
SysLimit1_1	System Limit 1	Input	BIT
↓	↓	Input	BIT
SysLimit1_10	System Limit 1	Input	BIT
SysLimit2_1	System Limit 2	Input	BIT
↓	↓	Input	BIT
SysLimit2_10	System Limit 2	Input	BIT
Out1MA	Feedback, Total output current, mA	Input	FLOAT
Out2MA	Feedback, Total output current, mA	Input	FLOAT

HART Signal Definitions

Each HART field device has a set of HART signals that are read from the field device. These signals are prefixed with either Hlx_ or HOx_ where x is 1-10 for input channels and 1-2 for output channels.

Signal	Type	Description
Hxx_CommCnt	Integer	Number of times the CommStat signal was not zero after a HART message
Hxx_CommStat	Bit encoded integer	HART Communication status Bit 1 – RX buffer overflow Bit 3 – Checksum error Bit 4 – Framing error Bit 5 – Overrun error Bit 6 – Parity error
Hxx_DevCnt	Integer	Number of times the DevStat signal was not zero after a HART message.
Hxx_DevStat	Bit encoded integer	Field Device Status: bits 0-7 Bit 0 – Primary variable out of limits Bit 1 – Non primary var out of limits Bit 2 – Analog output saturated Bit 3 – Analog output current fixed Bit 4 – More status available (ExStat) Bit 5 – Cold start Bit 6 – Configuration changed Bit 7 – Field device malfunction Command response byte: bits 8-15 2: Invalid selection requested 3: Passed parameter too large 4: Passed parameter too small 5: Too few bytes received

Signal	Type	Description
		6: Device specific device error 7: In write protect mode 8-15: Device specific 16: Access restricted 32: Device is busy 64: Command not implemented
Hxx_DevRev	Integer	Field Device - Device revision code as read from the device.
Hxx_HwSwRev	Integer	Byte 0 - Field device software revision Byte 1 - Field device hardware revision
Hxx_mA	Float	Field Parm 1 – current reading of the primary signal
Hxx_PV	Float	Field Device Specific Control Parm 2 - Primary field device value
Hxx_SV	Float	Field Device Specific Control Parm 3 - Secondary value
Hxx_TV	Float	Field Device Specific Control Parm 4 -Third value
Hxx_FV	Float	Field Device Specific Control Parm 5 -Fourth value

Extended Status Bits

The extended status bits are device-specific, and can be interrogated by using an AMS system. In general, the status bits are grouped as follows:

Bytes 0-5: Device specific status

Bytes 6-7: Operational modes

Bytes 8-10: Analog output saturation

Bytes 11-13: Analog output current fixed

Bytes 14-26: Device-specific

If needed, contact an authorized GE Representative for the appropriate Field Device documentation.

Each field device supports a specific number of control parameters and extended status bits. Refer to the *Field Device* documentation to determine the correct number and configure the ToolboxST application accordingly. A diagnostic alarm message will be generated if the Field Device and ToolboxST configuration do not match.

Hxx_ExStat_1	Bit Encoded	Extended Status Bytes 1-4
Hxx_ExStat_2	Bit Encoded	Extended Status Bytes 5-8
Hxx_ExStat_3	Bit Encoded	Extended Status Bytes 9-12
Hxx_ExStat_4	Bit Encoded	Extended Status Bytes 13-16
Hxx_ExStat_5	Bit Encoded	Extended Status Bytes 17-20
Hxx_ExStat_6	Bit Encoded	Extended Status Bytes 21-24
Hxx_ExStat_7	Bit Encoded	Extended Status Bytes 25-26